

## **ABSTRACT**

According to embodiments of the invention, multiple memory bus masters of a computer board are connected via transmission lines to a common node. The common node is further connected to a memory array. Each memory bus master can drive clock signals to the memory array. An isolation circuit is placed between the transmission lines and the common node. The isolation circuit is controllable to select one of the memory bus masters to drive clock signals to the memory array, while isolating the transmission lines of the other bus masters from the common node to reduce clock signal corruption.

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